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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/408,429	09/29/99	SANDORFI M	07072/086001

022494
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SUITE 101
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EXAMINER	
TRAN, D	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/408,429	Applicant(s) SANDORFI, MIKLOS	
	Examiner Denise Tran	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *13 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

DETAILED ACTION

1. Claims 1-19 are presented for examination.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19 of copending Application No. 09/408,807. Although the conflicting claims are not identical, they are not patentably distinct from each other. The claims of the current application do not have a controller for producing a control signal; however, both the concept and the advantages of providing a controller for producing a control signal are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to comprise a controller for producing a control signal because it would allow enhancing to the system controlling.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 recites the limitation "the main memory section" in lines 11-12. There is insufficient antecedent basis for this limitation in the claim.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandorfi, U.S. Patent No. 5768530.

As per claim 1, Sandorfi teaches the invention substantially as claimed, comprising: a semi conductor integrated circuit (e.g., fig. 1, el. 10); a data rebufferring section adapted to couple data from a one of a plurality of data ports to a data port of a processor selectively in accordance with

a control signal (e.g. figs. 4-5, els. 18 and 19; col.5, line 60 and et seq.); a main memory interface (e.g., fig.1, els 19,13, 17, 14) adapted for coupling to a main memory for the processor, such main memory interface being coupled to the data rebufferring section for providing control signals to the main memory section for enabling data transfer between the main memory and the processor through the data rebufferring section (e.g., col. 5, line 14 and et seq.). Sandorfi does not specifically teach the use of a microprocessor. "Official Notice" is taken that both the concept and the advantages of providing for a processor on a chip are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a processor on a chip to Sandorfi as a microprocessor because it would provide an increase in operating speed and a reduction of externally wired connection.

As per claims 2-4, 9-11, Sandorfi shows wherein a main memory is a selected one of a plurality of memory types (e.g., abstract) and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide data being transferred between the processor and the main memory through the main memory interface (e.g., col. 5, line 55); and one memory type is a RDRAM. Sandorfi does not explicitly show each memory type having a different data transfer protocol and the main memory interface is configured to provide a proper memory protocol to data being transferred. "Official Notice" is taken that both the concept and the advantages of providing for providing each memory type having a different data transfer protocol and a memory interface is configured to provide a proper memory protocol to data being transferred are well known and expected in the art. It would have

been obvious to one of ordinary skill in the art at the time the invention was made to include each memory type having a different data transfer protocol and a main memory interface is configured to provide a proper memory protocol to data being transferred because it would provide a memory interface for independently and flexibility supporting a plurality types of memories. Further more, Sandorfi does not explicitly show the use of SDRAM. Official Notice" is taken that both the concept and the advantages of providing SDRAM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a SDRAM because it would provide a faster operation in synchronous fashion.

As per claim 5-8, Sandorfi shows a circuit having a controller adapted for coupling to the main memory interface, such controller being adapted to produce a main memory access control signal (e.g., fig. 5, el. 19); the data rebufferring section including a selector responsive to the control signal for coupling data between a selected one of the data ports and the data port of the processor (e.g., figs. 4-5, els 63, 62); the data rebufferring section including a selector responsive to a control signal for coupling the data port of the processor to either :a selected one of data port; or the main memory (e.g., figs. 4-5, els 63, 62); a data distribution unit having a plurality of ports each one of the ports being coupled to a corresponding one of the selector, a RAM, an interrupt request controller, the processor port, and the main memory interface (e.g., figs. el 18 or 19). Sandorfi does not explicitly show a second integrated circuit adapted for controlling the first integrated circuit and the main memory has a two portion address locations, one portion being

addressed by the main memory interface in response to the processor and the other portion being addressed by the main memory interface in response to the controller. "Official Notice" is taken that both the concept and the advantages of providing a second integrated circuit separated from a first integrated circuit instead of one integrated circuit are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a second integrated circuit because it would minimize a cost to repair individual part instead of a whole circuit. "Official Notice" is taken that both the concept and the advantages of providing a meory with separate address portions for a different controller are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a memory with two portion address locations being addressed by two controllers because it would allow data processing independently and data integrity.

As per claims 12 and 19, Sandorfi shows the main memory interface comprising: a processor/main memory interface control section adapted to provide control signals between section and the processor and the controller (e.g., fig. 5, els 19,62-63). Sandorfi does not explicitly show each memory type having a different data transfer protocol and a main memory controller is configured to provide a proper memory protocol to data being transferred. "Official Notice" is taken that both the concept and the advantages of providing for providing each memory type having a different data transfer protocol and a memory controller is configured to provide a proper memory protocol to data being transferred are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was

made to include each memory type having a different data transfer protocol and a main memory interface is configured to provide a proper memory protocol to data being transferred because it would provide a memory interface for independently supporting a selected type of memory. Sandorfi does not explicitly show a mask to transform the address to an address in the second section of the memory. "Official Notice" is taken that both the concept and the advantages of providing for providing a mask to transform the address are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a mask to transform the address to Sandorfi because it would provide a selected group of bits of an address, thereby it allow independently, and flexibility supporting a different types of memory addresses portions..

8. Claims 13-18 would be allowable if a timely terminal disclaimer has been filed to overcome the Double Patenting rejections, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday and Thurs.. from 8.30 p.m. to 6.00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 308-3116. The fax phone number for this Group is (703) 305-9731 .

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

D.T

Denise Tran

03/24/01

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER